What is claimed is:

1. A liquid crystal display driver comprising:

a driving voltage generating circuit for generating first through fifth driving voltages and outputting the generated voltages via first through fifth output terminals;

a common/segment driving circuit, controlled by a driving polarity signal, for receiving the first through fifth driving voltages to generate a common driving signal and a segment driving signal;

a first capacitor connected between the first output terminal and a ground voltage;

a second capacitor;

a third capacitor; and

a control circuit for controlling connection of the output terminals and the capacitors in response to the driving polarity signal.

2. The liquid crystal display driver as claimed in claim 1, wherein the control circuit comprises:

a first switch for connecting one end of the second capacitor to one of the first output terminal and the fifth output terminal in response to the driving polarity signal;

a second switch for connecting the other end of the second capacitor to one of the second output terminal and the ground voltage in response to the driving polarity signal;

a third switch for connecting one end of the third capacitor to one of the second output terminal and the fourth output terminal in response to the driving polarity signal; and

a fourth switch for connecting the other end of the third capacitor to one of the third output terminal and the fifth output terminal in response to the driving polarity signal.

3. The liquid crystal display driver as claimed in claim 1, wherein the common/segment driving circuit generates the common driving signal and the segment driving signal using the first driving voltage, the fourth driving voltage, the fifth driving

voltage, and the ground voltage when the driving polarity signal is in a first logic state, and generates the common driving signal and the segment driving signal using the first driving voltage, the second driving voltage, the third driving voltage, and the ground voltage when the driving polarity signal is in a second logic state.

4. The liquid crystal display driver as claimed in claim 2, wherein when the driving polarity signal is in the first logic state, one end of the second capacitor is coupled to the fifth output terminal by the first switch, the other end of the second capacitor is coupled to the ground voltage by the second switch, one end of the third capacitor is coupled to the fourth output terminal by the third switch, and the other end of the third capacitor is coupled to the fifth output terminal by the fourth switch.

5. The liquid crystal display driver as claimed in claim 2, wherein when the driving polarity signal is in the second logic state, one end of the second capacitor is coupled to the first output terminal by the first switch, the other end of the second capacitor is coupled to the second output terminal by the second switch, one end of the third capacitor is coupled to the second output terminal by the third switch, and the other end of the third capacitor is coupled to the third output terminal by the fourth switch.

6. The liquid crystal display driver as claimed in claim 1, wherein the voltage difference between every two adjacent driving voltages among the first through fifth driving voltages is the same.

7. The liquid crystal display driver as claimed in claim 1, wherein the common/segment driving circuit comprises:

a common driving circuit, controlled by the driving polarity signal, for receiving the first driving voltage, the second driving voltage, the fifth driving voltage, and the ground voltage to generate the common driving signal; and

a segment driving circuit, controlled by the driving polarity signal, for receiving the first driving voltage, the third driving voltage, the fourth driving voltage, and the ground voltage to generate the segment driving signal.

8. The liquid crystal display driver as claimed in claim 7, wherein the common driving signal has the first driving voltage level and the fifth driving voltage level when the driving polarity signal is in a first logic state, and has the second driving voltage level and the ground voltage level when the driving polarity signal is in a second logic state.

9. The liquid crystal display driver as claimed in claim 7, wherein the segment driving signal has the fourth driving voltage and the ground voltage when the driving polarity signal is in a first logic state, and has the first driving voltage and the third driving voltage when the driving polarity signal is in a second logic state.

10. A liquid crystal display driver comprising:

a driving voltage generating circuit for generating first through fifth driving voltages to output the generated driving voltages via first through fifth output terminals;

a common/segment driving circuit, controlled by a driving polarity signal, for receiving the first through fifth driving voltages to generate a common driving signal and a segment driving signal;

a first capacitor connected between the first output terminal and a ground voltage;

a second capacitor;

a third capacitor;

a first switch for connecting one end of the second capacitor to one of the first output terminal and the fifth output terminal in response to the driving polarity signal;

a second switch for connecting the other end of the second capacitor to one of the second output terminal and the ground voltage in response to the driving polarity signal;

a third switch for connecting one end of the third capacitor to one of the second output terminal and the fourth output terminal in response to the driving polarity signal; and

a fourth switch for connecting the other end of the third capacitor to one of the third output terminal and the fifth output terminal in response to the driving polarity signal.

11. The liquid crystal display driver as claimed in claim 10, wherein the common/segment driving circuit generates the common driving signal and the segment driving signal using the first driving voltage, the fourth driving voltage, the fifth driving voltage, and the ground voltage when the driving polarity signal is in a first logic state, and generates the common driving signal and the segment driving signal using the first driving voltage, the second driving voltage, the third driving voltage, and the ground voltage when the driving polarity signal is in a second logic state.

12. The liquid crystal display driver as claimed in claim 10, wherein when the driving polarity signal is in a first logic state, one end of the second capacitor is coupled to the fifth output terminal by the first switch, the other end of the second capacitor is coupled to the ground voltage by the second switch, one end of the third capacitor is coupled to the fourth output terminal by the third switch, and the other end of the third capacitor is coupled to the fifth output terminal by the fourth switch.

13. The liquid crystal display driver as claimed in claim 10, wherein when the driving polarity signal is in a second logic state, one end of the second capacitor is coupled to the first output terminal by the first switch, the other end of the second capacitor is coupled to the second output terminal by the second switch, one end of the third capacitor is coupled to the second output terminal by the third switch, and the other end of the third capacitor is coupled to the third output terminal by the fourth switch.

14. The liquid crystal display driver as claimed in claim 10, wherein the voltage difference between every two adjacent driving voltages among the first through fifth driving voltages is the same.

15. The liquid crystal display driver as claimed in claim 10, wherein the common/segment driving circuit comprises:

a common driving circuit, controlled by the driving polarity signal, for receiving the first driving voltage, the second driving voltage, the fifth driving voltage, and the ground voltage to generate the common driving signal; and

a segment driving circuit, controlled by the driving polarity signal, for receiving the first driving voltage, the third driving voltage, the fourth driving voltage, and the ground voltage to generate the segment driving signal.

16. The liquid crystal display driver as claimed in claim 15, wherein the common driving signal has the first driving voltage level and the fifth driving voltage level when the driving polarity signal is in a first logic state, and has the second driving voltage level and the ground voltage level when the driving polarity signal is in a second logic state.

17. The liquid crystal display driver as claimed in claim 15, wherein the segment driving signal has the fourth driving voltage level and the ground voltage level when the driving polarity signal is in a first logic state, and has the first driving voltage level and the third driving voltage level when the driving polarity signal is in a second logic state.

18. A method for reducing the number of capacitors for driving voltage stabilization in a liquid crystal display driver including a driving voltage generating circuit for generating first through fifth driving voltages and outputting the generated voltages via first through fifth output terminals, and a common/segment driving circuit, controlled by a driving polarity signal, for receiving the first through fifth driving voltages to generate a common driving signal and a segment driving signal, the method comprising:

connecting a first capacitor between the first output terminal and a ground voltage;

when the driving polarity signal is in a first logic state, connecting one end of a second capacitor to the fifth output terminal by a first switch, connecting the other end of

the second capacitor to the ground voltage by a second switch, connecting one end of a third capacitor to the fourth output terminal by a third switch, and connecting the other end of the third capacitor to the fifth output terminal by a fourth switch; and

when the driving polarity signal is in a second logic state, connecting one end of the second capacitor to the first output terminal by the first switch, connecting the other end of the second capacitor to the second output terminal by the second switch, connecting one end of the third capacitor to the second output terminal by the third switch, and connecting the other end of the third capacitor to the third output terminal by the fourth switch.

19. The method as claimed in claim 18, wherein the common/segment driving circuit generates the common driving signal and the segment driving signal using the first driving voltage, the second driving voltage, the third driving voltage, and the ground voltage when the driving polarity signal is in the first logic state, and generates the common driving signal and the segment driving signal using the first driving voltage, the fourth driving voltage, the fifth driving voltage, and the ground voltage when the driving polarity signal is in the second logic state.

20. The method as claimed in claim 18, wherein the voltage difference between every two adjacent driving voltages among the first through fifth driving voltages is the same.